CLAIMS

Now, therefore, the following is claimed:

1. A multiplexor circuit, comprising:

a plurality of data connections;

first stage logic configured to receive a first data word from one of the connections and to transmit the first data word received; and

second stage logic configured to receive the first data word from the first stage logic and to select a selected data word between the first data word and a second data word received from another of the plurality of data connections based upon a set of select signals, the second stage logic configured to transmit the selected data word.

2. The circuit of claim 1, wherein the second stage logic is further configured to transmit the selected data word to a third stage logic.

3. The circuit of claim 1, wherein the second stage logic is further configured to transmit the selected data word to a system bus.

4. The circuit of claim 2, wherein the second logic is further configured to increase signal strength of the first data word when the first data word is transmitted, if the first data word is selected.

5. The circuit of claim 2, wherein the second stage logic comprises:

a first tristate driver configured to drive a connection with the first data word from the first stage logic, the first tristate driver enabled if a data connection exclusion signal is asserted and disabled if the data connection exclusion signal is deasserted;

a second tristate driver configured to drive the connection with the second data word, the second tristate driver enabled if a data connection select signal is asserted and disabled if the data connection selection signal is deasserted.

6. The circuit of claim 5 wherein the first tristate driver increases the signal strength of the first data word when the selected data word is the first data word.

7. The circuit of claim 5, further comprising:

a first latch circuit configured to receive the data connection exclusion signal, the first latch circuit configured to latch the value indicative of the data connection exclusion signal at an output of the first latch circuit, the output of the first latch circuit configured to enable the first tristate driver if the data connection exclusion signal is asserted;

a second latch circuit configured to receive the data connection selection signal, the second latch circuit configured to latch the value indicative of the data connection selection signal at an output of the second latch circuit, the output of the second latch circuit configured to enable the second tristate driver if the data connection selection signal is asserted;

a third latch circuit configured to receive the second data word, the third latch circuit configured to latch the second data word at an output of the third latch circuit, the output of the third latch circuit configured for receipt by the second tristate driver;

a first clock configured to transmit a clock signal to the first, second, and third latch circuits, the clock signal activating latching of the second data word, the data connection selection signal and the data connection exclusion signal at the outputs of the third, second and first latch circuits, respectively.

8. A circuit comprising

a plurality of data connections;

logic associated with a first data connection of the plurality of data connections, the logic associated with the first data connection configured to transmit a first data word corresponding to the first data connection;

logic associated with a second data connection of the plurality of data connections configured to receive the first data word corresponding to the first data connection from the logic associated with the first of the plurality of data connections, the logic associated with the second data connection configured to select a first selected data word between the first data word and a second data word corresponding to the second data connection based upon a set of select signals; and

logic associated with a third data connection of the plurality of data connections configured to receive the first selected signal set, the logic associated with the third data connection configured to select a second selected data word between the first data word and a third data word corresponding to the third data connection based upon a set of select signals, the logic associated with the third data connection further configured transmit the second selected data word to a system bus.

9. A multiplexor circuit, comprising:

a first tristate driver comprising a first data input, a first data output, and a first enable input, the first tristate driver adapted to receive a first data word via the first data input representative of a first data connection;

a second tristate driver comprising a second data input, a second data output, and a second enable input, the second tristate driver adapted to receive a second data word representative of a second data connection;

a connection adapted to receive, via the data output of the first tristate driver, the first data word, if a first signal is asserted at the first enable input of the first tristate driver, the connection further adapted to receive, via the second data output of the second tristate driver, the second data word, if a second signal is asserted at the enable input of the second tristate driver.

10. The multiplexor circuit of claim 9, further comprising select logic configured to assert the first signal if an application program desires the first data word representative of the first data connection and configured to assert the second signal if the application program desires the second data word representative of the second data connection.

11. The multiplexor circuit of claim 10, wherein the select logic deasserts the first signal if the application program does not desire the first data word and deasserts the second signal if the application program does not desire the second data word.

12. The multiplexor circuit of claim 11, wherein the first signal and the second signal enable and disable the first and second tristate drivers simultaneously.

13. The multiplexor circuit of claim 12, further comprising:

a first latch circuit configured to transmit the first signal to the first tristate driver upon a leading edge of a clock signal; and

a second latch circuit configured to transmit the second signal to the second tristate driver upon the leading edge of the clock signal.

14. A method for distributing multiplexing, comprising

means for receiving a first data word corresponding to a first data connection;

means for transmitting the first data word to first logic associated with a second data connection;

means for selecting a selected data word via the first logic between the first data word and a second data word transmitted from the second data connection based upon a set of select signals; and

means for transmitting the selected data word.

15. A method for distributing multiplexing, comprising

receiving a first data word corresponding to a first data connection;

transmitting the first data word to first logic associated with a second data connection;

selecting a selected data word via the first logic between the first data word and a second data word transmitted from the second data connection based upon a set of select signals; and

transmitting the selected data word.

16. The method of claim 15, wherein the selected data word is transmitted to a discrete integrated circuit (IC) component.

17. The method of claim 16, wherein the select signals comprise a data connection selection signal indicative of which data word is to be selected and a data connection exclusion signal indicative of which data word is to be excluded.

18. The method of claim 15, wherein the selecting step comprises:

driving the second data word to a connection via a first tristate driver if the data connection selection signal is asserted; and

disabling a second tristate driver configured to receive the first data word and configured to drive the first data word to the connection if the data connection exclusion signal is asserted.

19. The method of claim 18, wherein the selecting step further comprises:

driving the first data word to the connection via the second tristate driver if the data connection exclusion signal is asserted; and

disabling the first tristate driver if the data connection selection signal is deasserted.

20. The method of claim 19, wherein the driving the first data word to the connection further comprises increasing signal strength of the first data word.